REMARKS

Claims 1-14, 23-26, and 31-44 are pending.

Claim 38 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In particular, the Examiner indicated that there was not antecedent bases for "the first zone" and "the second zone" in the last four lines of claim 38. The applicant submits that the Examiner is mistaken. Claim 38 depends on claim 34 which recites "a first zone" and "a second zone" in the last three lines of the claim. Thus, claim 38 particularly points out and distinctly claims the invention.

Claims 1-14, 23-26, 31-32, and 24-43 were rejected under 35 U.S.C. § 103 as being unpatentable over United States Patent No. 6,127,723 to Aiello et al. ("Aiello") in view of U.S. Patent No. 6,207,481 to Yi et al. ("Yi").

The cited prior art does not teach or suggest the invention recited in the pending claims. For example, claim 1 recites an integrated device that includes a quenching element having a Zener diode made in polysilicon and formed on a second surface of a semiconductor chip and comprising a polysilicon layer having at least one zone of the first conductivity type and at least one zone of a second conductivity type in order to form at least one P-N junction. Aiello and Yi do not teach or suggest such a quenching element connected as recited in claim 1, for at least three reasons.

First, there is no motivation to combine Aiello with Yi to produce the claimed invention. Aiello shows a diode D1 formed in a monocrystalline epitaxial layer 218 while Yi shows a thin film transistor formed in a polysilicon layer 218. Nothing in Aiello, Yi, or the general knowledge of the prior art provides a reason to replace the monocrystalline diode D1 with the thin film transistor of Yi.

The Examiner incorrectly asserts that Yi teaches that using polysilicon results in a uniform crystal size and better transistor performance. This assertion is both unsupported by any statement in Yi and is factually incorrect. A primary basis of the entire semiconductor industry is that a transistor integrated in a single crystal of silicon provides better transistor performance than a transistor formed in a polysilicon layer. If that were not true, then semiconductor companies would not need to spend the time and expense producing monocrystalline silicon

chips. Further, by definition, a single crystal of silicon has a perfectly uniform crystal size because there is only one crystal size, and thus, Yi's polysilicon could not possibly have a more uniform crystal size. Rather than comparing polysilicon to monocrystalline silicon, as in Aiello, Yi simply reports that the method of producing a polysilicon layer in Yi is better than prior art methods of producing polysilicon layers. If the Examiner continues to make the assertion that Yi reports that using polysilicon results in advantages over moncrystalline silicon, the applicant requests that the Examiner point to some statement in Yi that supports the assertion.

In response to applicants' explanation of the lack of motivation for combining Aiello with Yi, the Examiner responded that "case laws make it clear that choosing an appropriate material is in fact within the level of ordinary skill in the art." This assertion by the Examiner is unsupported and not true. There is no case law stating or implying that choosing an appropriate material is always within the skill of the art. It is clearly true that if the prior art teaches away from employing a particular material, then it would not be within the ordinary skill in the art to use that particular material. Moreover, the claimed invention does not merely change materials from a monocrystalline substrate to a polysilicon layer – instead, an entirely new polysilicon layer is added on top of a monocryalline substrate.

For the foregoing reasons, there is no suggestion or motivation for combining Ti with Aiello as suggested by the Examiner.

Second, even if one were motivated to combine Yi with Aiello, one still would not create the claimed invention. Claim 1 recites a device that includes a polysilicon quenching on a surface of a semiconductor chip that includes first and second transistors. In contrast, Aiello teaches incorporating all of the active elements in a single monocrystalline silicon chip 200 and Yi teaches incorporating a transistor in a polysilicon layer above a glass substrate that does not incorporate any active elements. As such, even if the Examiner were correct that Yi teaches the use of polysilicon rather than monocrystalline silicon, then one would at best put all of the active elements of Aiello in polysilicon. Nothing in Aiello or Yi suggest putting one element in polysilicon and the other elements in a monocrystalline silicon substrate. Thus, even a hypothetical combination of Aiello and Yi would not result in the claimed invention.

Third, even if one were motivated to employ the thin film transistor of Yi on the structure of Aiello, one still would not create the claimed invention. Claim 1 recites that the quenching element, which includes a polysilicon PN junction, is coupled with the base region of the first transistor and with the not drivable terminal of the second transistor. Neither Aiello nor Yi suggest connecting a polysilicon PN junction to a base region or not drivable terminal of integrated transistors. In particular, Yi does not connect the thin film transistor of layer 118 to any regions or terminals of any transistors in the substrate 111. Thus, a hypothetical combination of Yi with Aiello would at most merely position the thin film transistor of Yi in a polysilicon layer above the structure of Aiello, without connecting the thin film transistor as a quenching element between the base terminal of a first transistor and a not drivable terminal of a second transistor.

The Examiner responded simply by noting that the diode D1 of Aiello is connected to the transistors Td1 and Td2, without explaining why one would not simply position the thin film transistor of Yi to the top of Aiello. The Examiner seems to believe that, merely because Yi shows a polysilicon transistor above a glass substrate, one would somehow be motivated to choose to move only the diode D1 of Aiello into a polysilicon layer while still maintaining the same connections. The Examiner also does not explain why the person of ordinary skill would not merely move the transistor Td1 into a polysilicon layer while keeping the diode D1 in the monocrystalline substrate. It appears that the Examiner is improperly using hindsight to pick and choose among the teachings of the prior art based solely on the applicant's disclosure.

For the foregoing reasons, claim 1 is nonobvious in view of the cited prior art.

Claims 2-14, and 31 depend on claim 1, and thus, are likewise nonobvious in view of the cited prior art.

Although the language of claims 23-26, 32, and 34-43 differs from that of claims 1-14, and 31, the allowability of claims 23-26, 32, and 34-43 will be apparent in view of the above discussion.

Claims 33 and 44 were rejected under 35 U.S.C. § 103 as being obvious in view of Aiello, Yi, and U.S. Patent No. 4,994,880 to Kato *et al.* ("Kato").

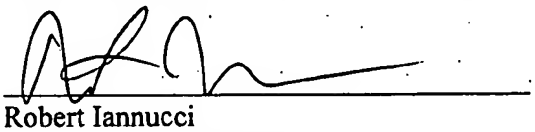
The cited prior art does not teach or suggest the invention recited in claims 33 and 44. First, Kato does not teach or suggest the features mentioned above with respect to claims 1 and 34, from which claims 33 and 44 respectively depend. Second, the cited art does not teach or suggest the addition features recited in claims 33 and 44. In particular, claims 33 and 44 recite a plurality of zener diodes distributed along the perimeter of elongated portions of an emitter region of a first transistor. The Examiner points to Figure 8A of Kato as showing an emitter surface electrode 47 in a comb shape, but does not point to even a single zener diode positioned along the perimeter of the electrode 47. Aiello is the only cited reference that shows any zener diodes, but Aiello does not show plural zener diodes in any embodiment and does not suggest plural zener diodes along the perimeter of an emitter region. Accordingly, claims 33 and 44 are nonobvious in view of the cited prior art.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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